NWEI Wave Energy Demonstration at the Navy's WETS 30m Project Site

2014

Test Report - Low Power Testing of Grid Interconnection System

Northwest Energy Innovations

10/31/2014

Table of Contents

1. Introduction

This document describes low power testing of the 30m Wave Energy Test Site (WETS) grid interconnection infrastructure that has been installed by NWEI in Room 106 of Battery French (Building 614) at Marine Corps Base Hawaii (MCBH). This equipment will be used to operate the NWEI half-scale device at the 30 m site. This testing was conducted in order to validate operation of the grid interconnection inverters, inverter control system, electrical infrastructure, onshore data acquisition, and communications equipment before the NWEI device is deployed. This equipment was installed and tested in October 2014.

2. Test Plan

The NWEI document "Test Plan for Low Power Testing of Grid Interconnection System" is included in Appendix I of this document. Included in this test plan is a description of the equipment tested, test objectives, test setups, test instrumentation, and detailed plans describing the specific tests performed. Tests were conducted per this test plan except where noted in this report.

3. Description of the Equipment Tested

See Figure 1 for a diagram of the complete electrical and grid interconnection system for the half-scale NWEI device. The grid interconnection equipment shown in the right-center of Figure 1 was installed in Room 106 of Building 614 in October 2014. Low power testing of this equipment is described in report. A photograph of this equipment, installed on the west wall of Room 106, is shown in Figure 2. Photographs of the insides of four custom enclosures used in the installation are shown in Figures 3-6. Detailed electrical drawings for this equipment are included in Appendix II. See the NWEI document *Design Report: Interconnection of a 20kW Wave Energy Device at the WETS 30m Site* for a detailed description of this system.

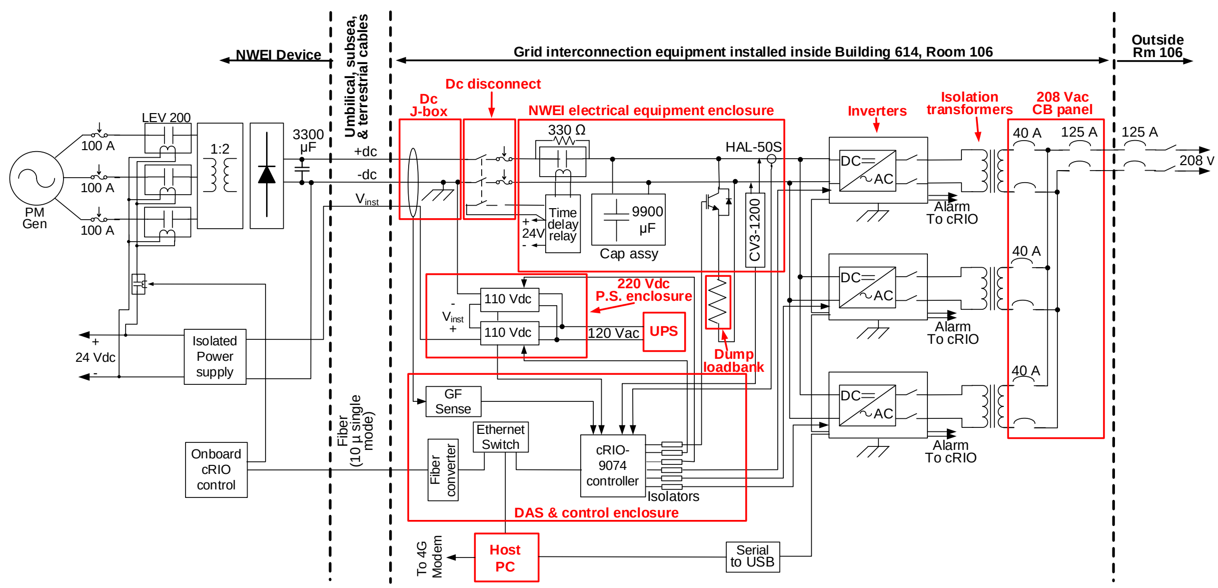

Figure 1 Overview of NWEI electrical power and grid interconnection system

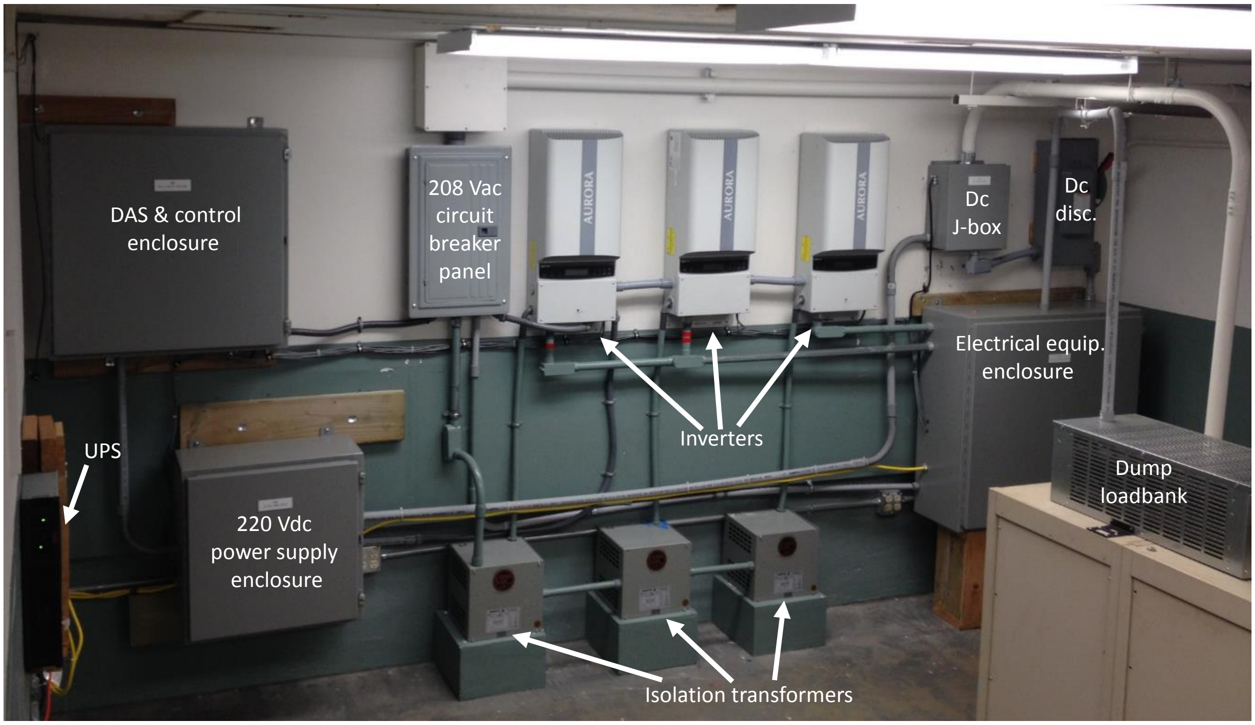

Figure 2 NWEI installed grid interconnection equipment on west wall of Room 106

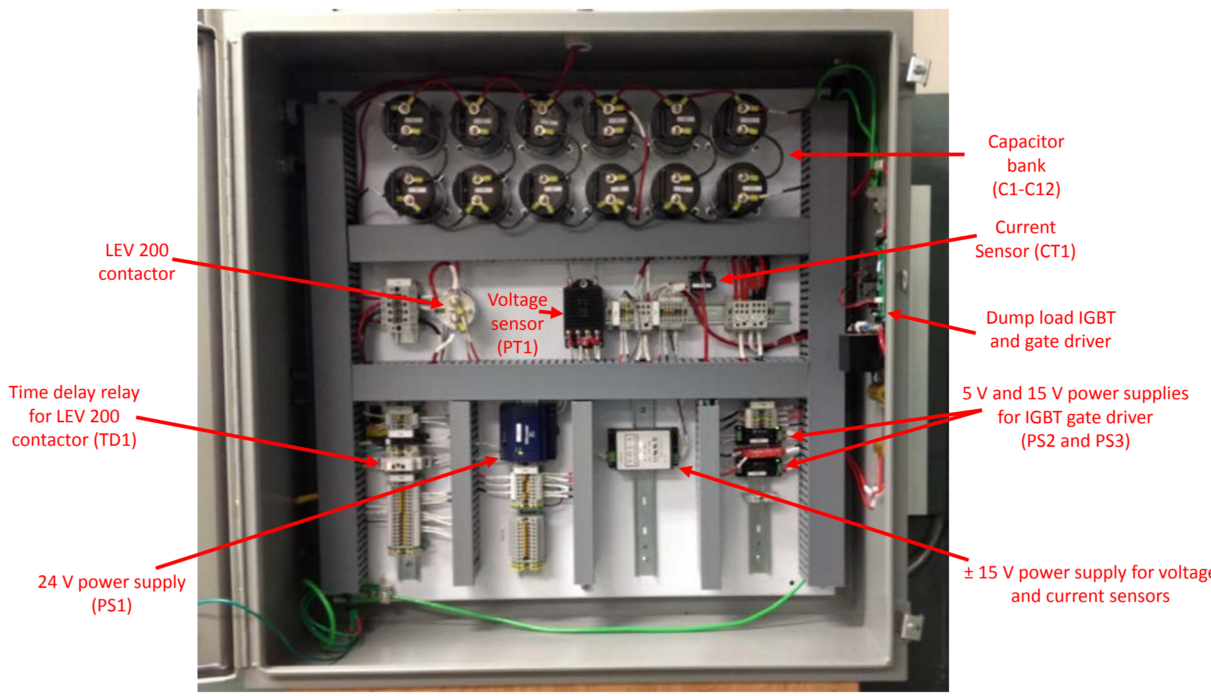

Figure 3 NWEI electrical equipment enclosure

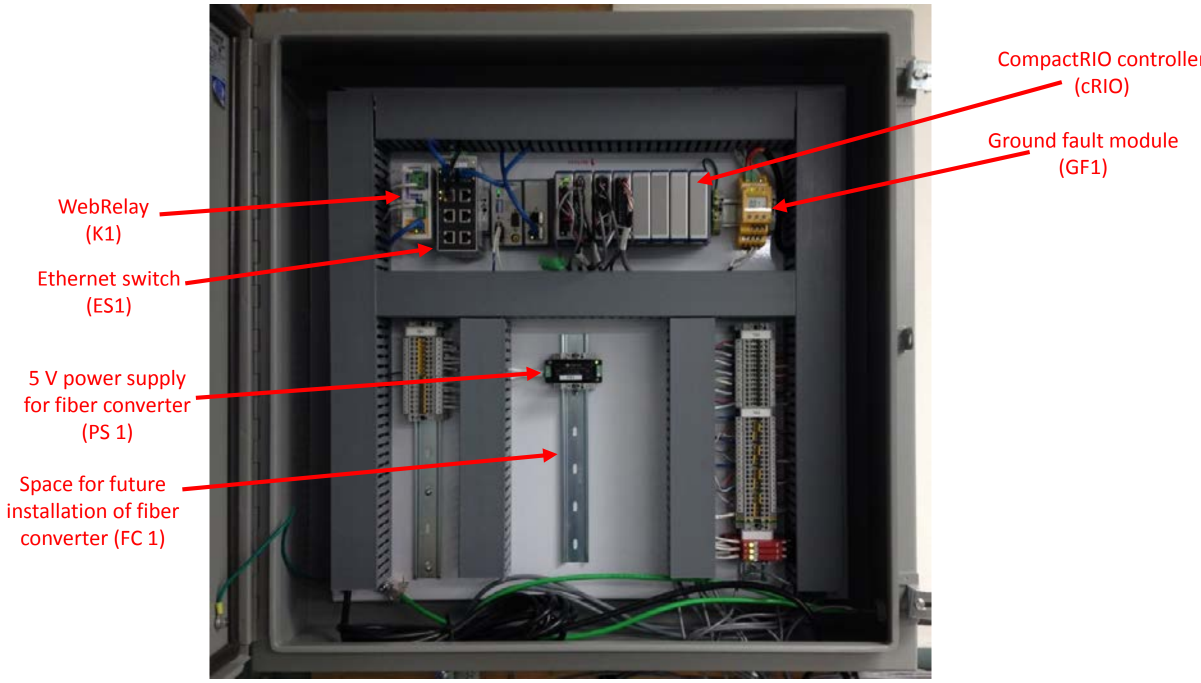

Figure 4 NWEI DAS and control enclosure

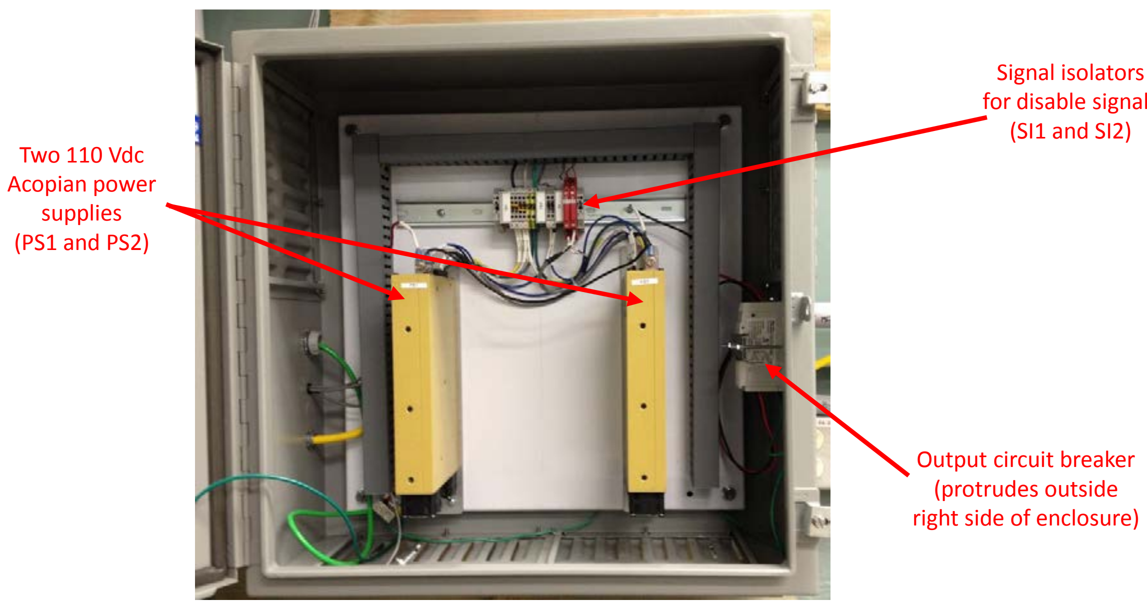

Figure 5 NWEI 220 Vdc power supply enclosure

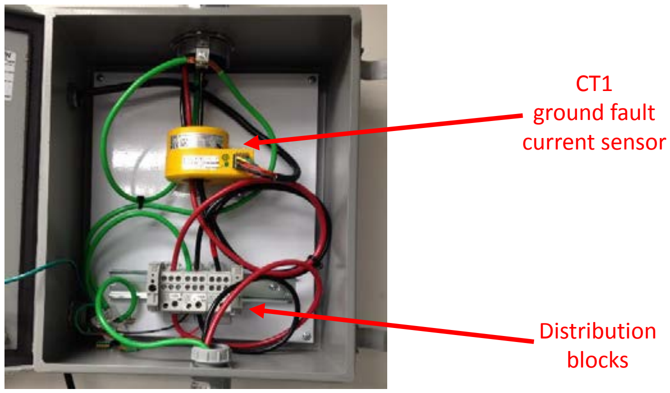

Figure 6 NWEI dc junction box

Figure 7 shows a photograph of the host PC located at the east end of Room 106. This PC primarily serves as the user interface for two National Instruments CompactRIO (cRIO) controllers, one to be located offshore in the NWEI device and one located in the NWEI DAS enclosure on the west wall of Room 106. These control the NWEI device and the grid interface equipment in Room 106. At the time these tests were performed, the offshore cRIO was not connected to the system. This interface uses custom LabVIEW software developed by NWEI. The host PC can also interface directly with the three inverters on the west wall of Room 106 using Aurora Installer software provided by the inverter manufacturer, PowerOne.

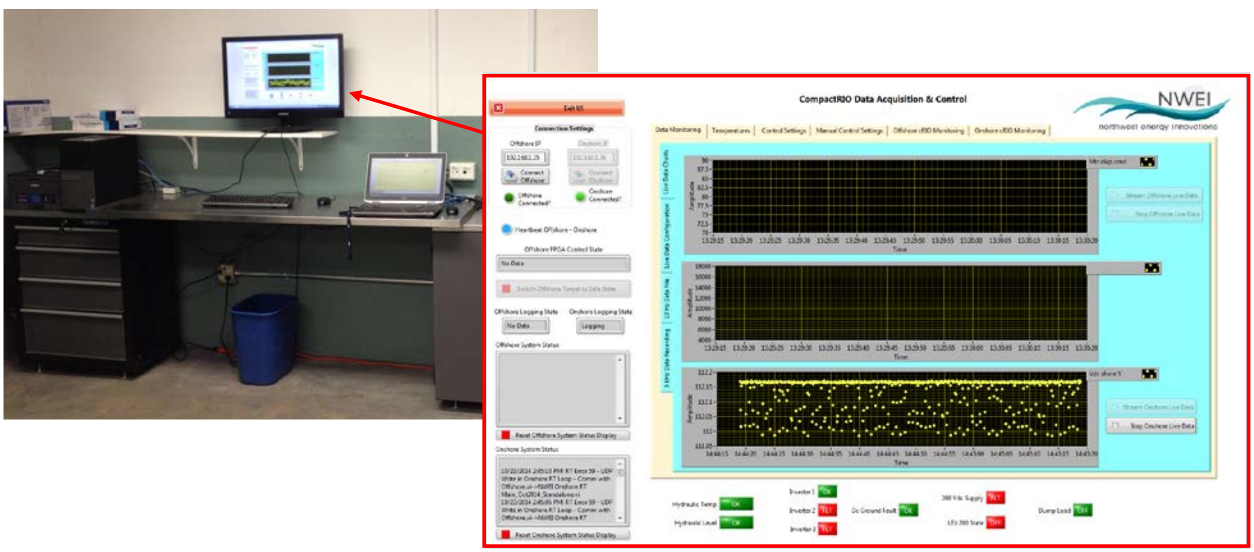

Figure 7 Host PC at the east side of Room 106 and the NWEI cRIO user interface

4. Test Results

Low power testing of the grid interconnection equipment in Room 614 was performed using the test setups and test procedures described in the test plan, included in Appendix II; refer to that appendix for that information.

4.1. UPS and 24 Vdc power supply tests

The UPS and power supply tests were conducted per Section 5.1 of the test plan (Appendix I).

4.1.1. *UPS and power supply voltage measurements*

UPS and power supply voltage measurements were made per steps 2-4 of test plan Section 5.1. All measurements were made with a Fluke 15B digital voltmeter. The results are shown in Table 1; all measurements were within expected ranges.

Table 1 UPS and power supply voltage measurements

Test Procedure Step	Measurement
2. UPS output at no load	120.5 V
3. 24 Vdc power supply output (PS1) electrical equipment enclosure	24.12
4. Electrical equipment enclosure PS2 output voltage	24.11 V
Electrical equipment enclosure PS3 output voltage	24.11 V
Electrical equipment enclosure PS4 output voltage	24.11 V
DAS enclosure K1 output voltage	24.06 V
DAS enclosure cRIO input voltage	24.05 V
DAS enclosure GF1 input voltage	24.06 V
DAS enclosure ES1 input voltage	24.06V
DAS enclosure PS1 output voltage	24.06V
5. Electrical equipment enclosure PS2 output	5.00 V
Electrical equipment enclosure PS3 output	15.01 V
Electrical equipment enclosure PS4 output	+15.02/-15.06 V
DAS enclosure PS2 output PS1 output	5.00 V

4.1.2. *Functionality of Schneider time delay relay and LEV200 contactor*

This test was conducted per Section 5.1, Step 6 of the test plan. Resistance measurements were made with a Fluke 15B meter and time measurements were made with an Iphone stopwatch. With the dc disconnect open, the resistance measured across the LEV200 contacts was 327 Ω (expected approximately 330 Ω). After the disconnect was closed, there was a 61 s delay then the LEV200 contactor closed (expected approximately 60 s delay). The resistance across the closed LEV 200 contacts was 0 Ω as expected.

4.1.3. *Functionality of CompactRIO-9074 controller*

Basic functionality of the cRIO controller was verified with the host PC user interface.

4.1.4. *UPS tests*

The UPS was tested per Section 5.1, Steps 8 and 9 of the test plan. A photograph of the setup used is shown in Figure 8. A work light with a 500 W bulb was used to simulate future loading of the offshore equipment through the 220 Vdc power supply (after the NWEI device is deployed). The 220 Vdc power supply was disconnected from the UPS for this test. The electrical equipment enclosure was connected to the UPS output in its normal configuration. The tests were performed after the UPS had been charged for over 12 hours. In order to measure the UPS holdup time without continuously monitoring the UPS output, the input to the UPS was unplugged and the data logging time of the cRIO controller was recorded at that moment. When the UPS shut down at the end of its holdup time, power was lost to the cRIO and data logging stopped, so that the UPS shut down time could be determined from the time recording for the last entry of the cRIO data.

Figure 8 Photo of UPS test setup

The results of the UPS tests are shown in Table 2. The UPS holdup time was approximately 37 minutes when the test was performed per the test plan with the host PC independently powered. This exceeded the design goal of 15 minutes holdup. A second test was run the following day to measure the effect of adding the host PC to the UPS output. Although powering the host PC from the UPS was not anticipated earlier, reconfiguring the system this way is preferred because it will reduce nuisance shutdowns of the host PC during power interruptions. Because the host PC will be remotely operated, shutdowns will be inconvenient. The results of the second test show that the UPS holdup was 33 minutes when the host PC is powered by the UPS. This still far exceeds the 15 minute design goal, so the host computer will be powered by the UPS during deployment.

Table 2 UPS test results

Test condition	Time UPS input power disconnected	Time UPS output power switched off	Elapsed time (min)
UPS load: - Electrical equip. enclosure - 500 W light (simulates offshore load)	10/23/2014 23:32:00 UTC	10/23/2014 24:08:50 UTC	36:50
UPS load: - Electrical equip. enclosure - 500 W light (simulates offshore load) - Host PC	10/24/2014 19:33:00 UTC	10/24/2014 20:06:00 UTC	33:00

4.2. 220 Vdc power supply tests

The 220 Vdc power supply tests were conducted per Section 5.2 of the test plan (Appendix I).

4.2.1. *Output voltage*

The no load output voltage of the 220 Vdc power supply was measured at the terminals in the dc j-box with a voltmeter as shown in Figure 9. The voltage was 219.5 Vdc.

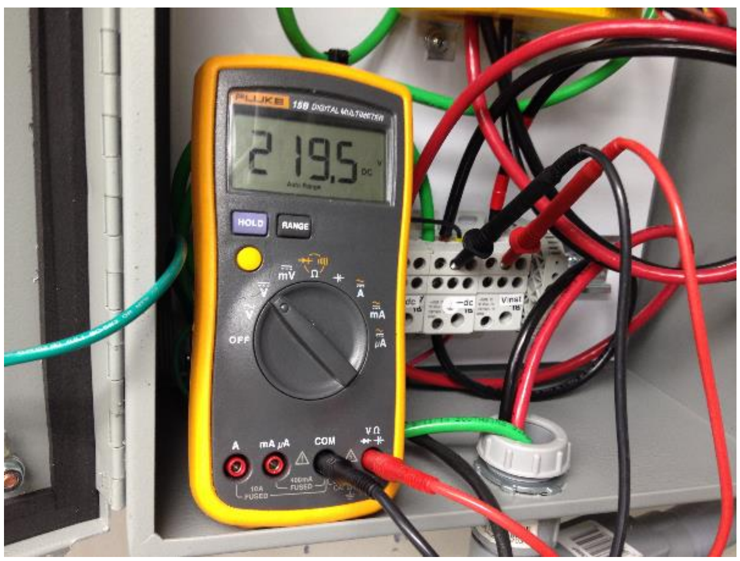

Figure 9 Measurement of 220 Vdc power supply voltage

4.2.2. *Alarm and shorted output*

Proper operation of the Acopian power supply alarm outputs and the ability of the two series 110 V power supplies that provide 220 Vdc power to withstand shorted outputs was verified as shown in Figure 10. The power supply inputs were disconnected, and the shorting wire connected to the 220 Vdc output. Input power was reconnected. The 220 Vdc power supply alarm indicator at the bottom of the cRIO user interface, shown in Figure 10, indicated a fault. The power supply inputs were again disconnected, the shorting wire removed, and the inputs reconnected. The 220 Vdc power supply fault was no longer indicated by the user interface and output voltage returned to normal.

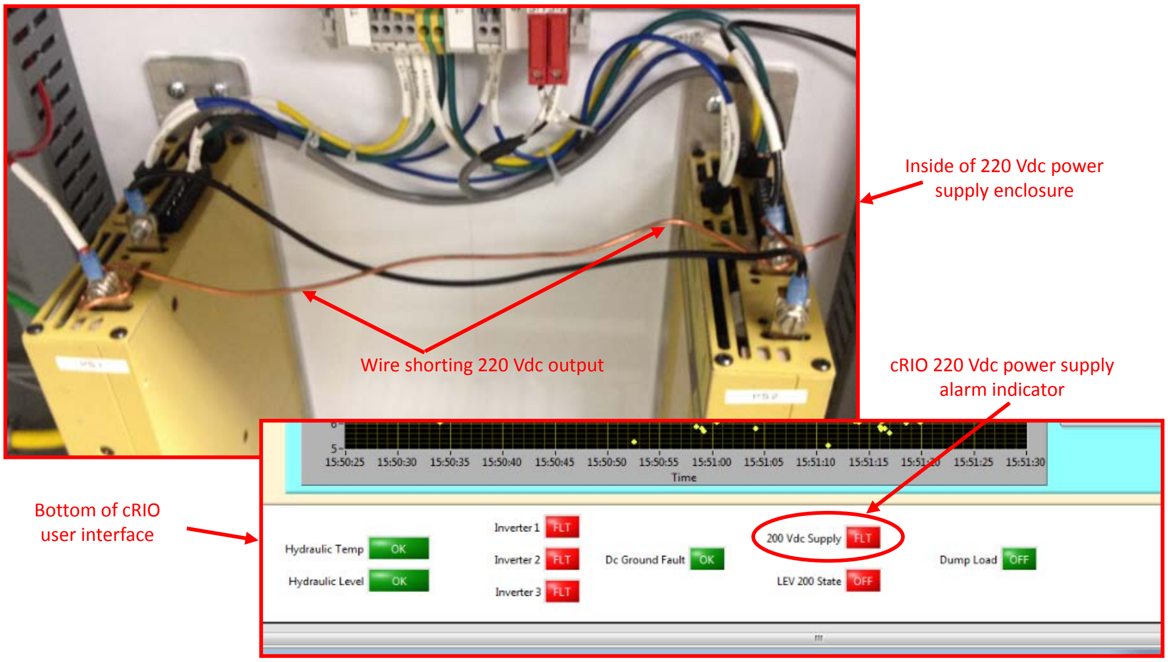

Figure 10 Test setup for output shorting of 220 Vdc power supply

4.2.3. *220 Vdc power supply disable via CompactRIO controller*

After verifying correct output voltage from the 220 Vdc supply with no fault indication, the power supply disable switch on the host PC user interface was activated. The power supply output voltage, measured with a voltmeter, switched to 0.05 V and a 220 Vdc power supply fault was indicated on the user interface. See Figure 11 for a screen shot of the user interface at this time. The disable switch was then deactivated and both the output voltage and fault indicator returned to normal states.

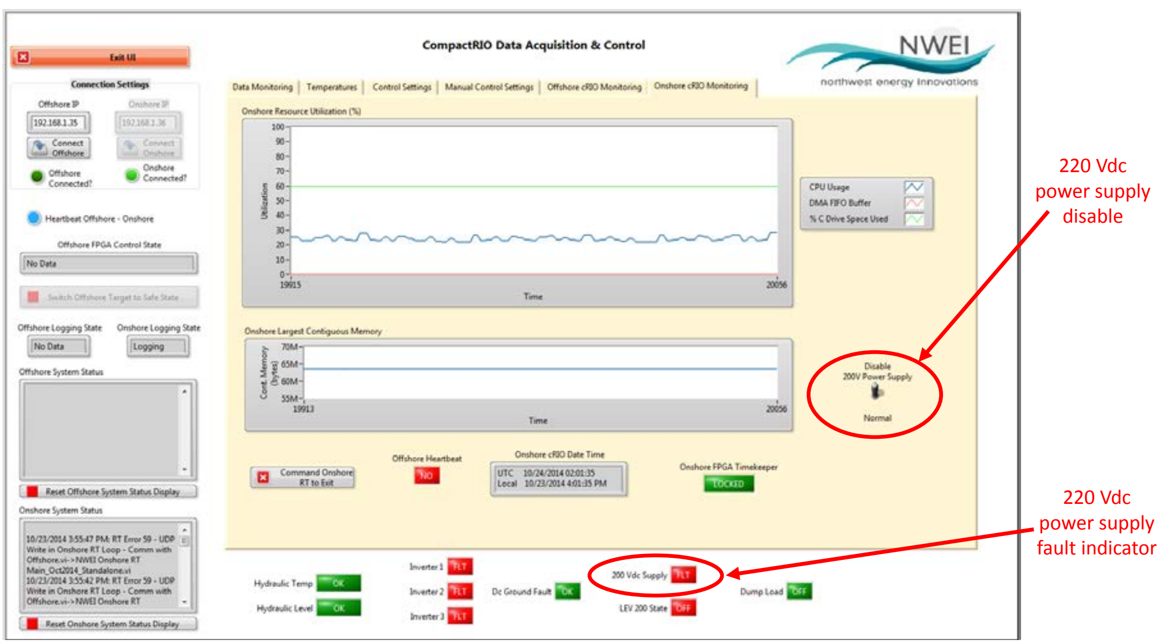

Figure 11 CompactRIO host user interface showing disable of 220 Vdc power supply

4.3. Inverter configuration and low power testing

These tests were conducted per Section 5.3 of the test plan (Appendix I).

4.3.1. *Inverter configuration*

The three inverters were configured using the user interface on the inverters themselves as well as Aurora Installer software installed on the host PC as described in Section 5.3, Steps 1-4 of the test plan. The host PC is connected to the three inverters through a RS-485 serial link. The Aurora Installer software was provided by the inverter manufacturer PowerOne.

The Aurora Installer software was used to program the three inverters with identical 30-150 Hz, 0-6 kW linear output power versus frequency curves, consistent with CompactRIO software. The nominal grid voltage of the three inverters was set to 208 V using their front panel user interfaces. See Figure 12 for a screen shot of the Aurora Installer “wind configuration” window for Inverter 1, showing the P vs f curve and 208 V nominal grid setting. This screen also shows the 66 Vdc input voltage from a variable dc power supply connected to their inputs and the 30 Hz control signal frequency that existed at the time the inverters were configured. This Aurora Installer window was identical for the other two inverters.

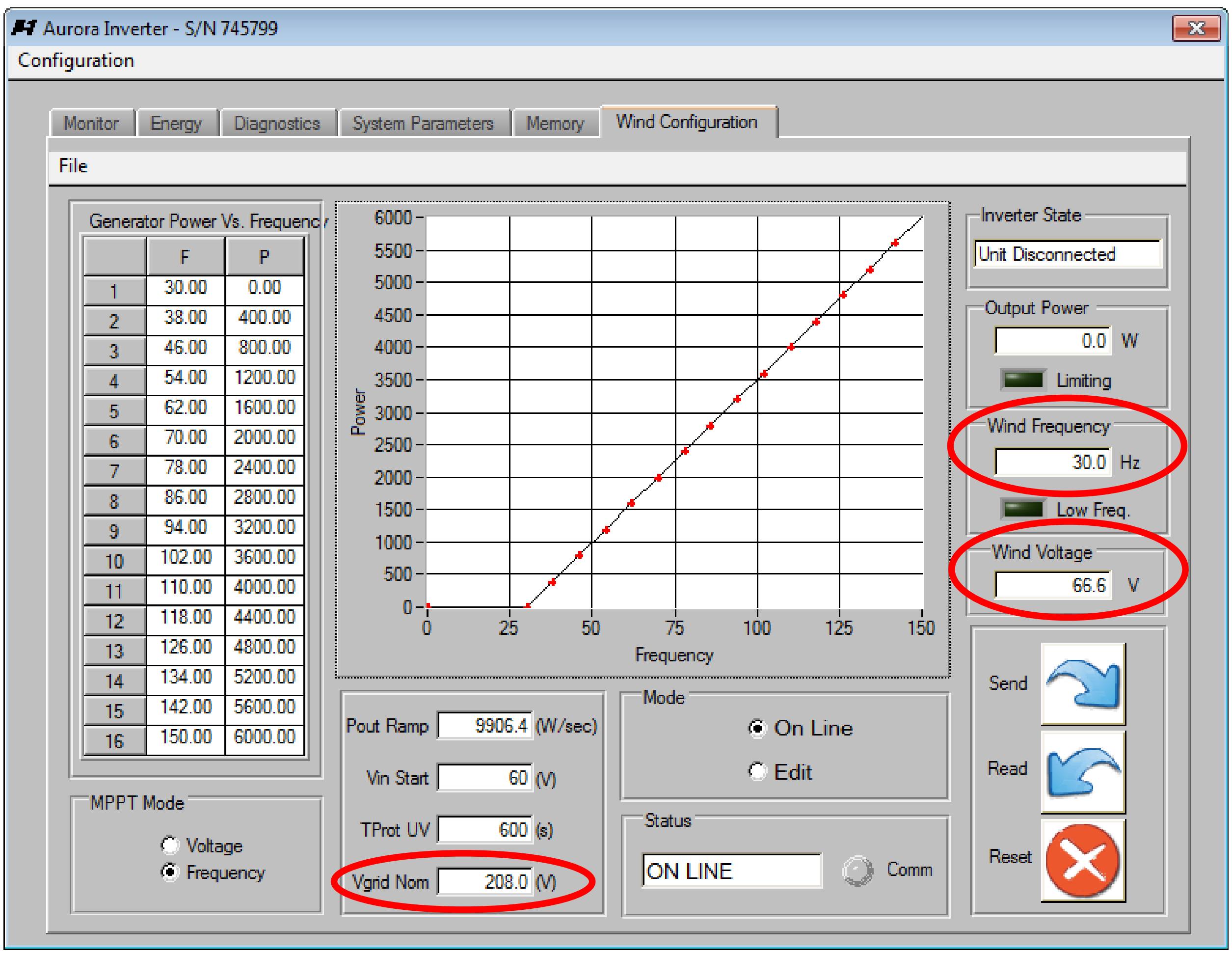

Figure 12 Aurora Installer wind configuration window

The Aurora Installer software was also used to disable the isolation resistance fault detection in the three inverters per Section 5.3, Step 4 of the test plan. See Figure 13 for a screen shot of the Aurora Installer "System Parameters" window for Inverter 1 that shows the isolation resistance detection disabled. This Aurora Installer window was identical for the other two inverters. The isolation resistance detection must be disabled for multiple PowerOne inverters to operate in parallel, per PowerOne guidelines.

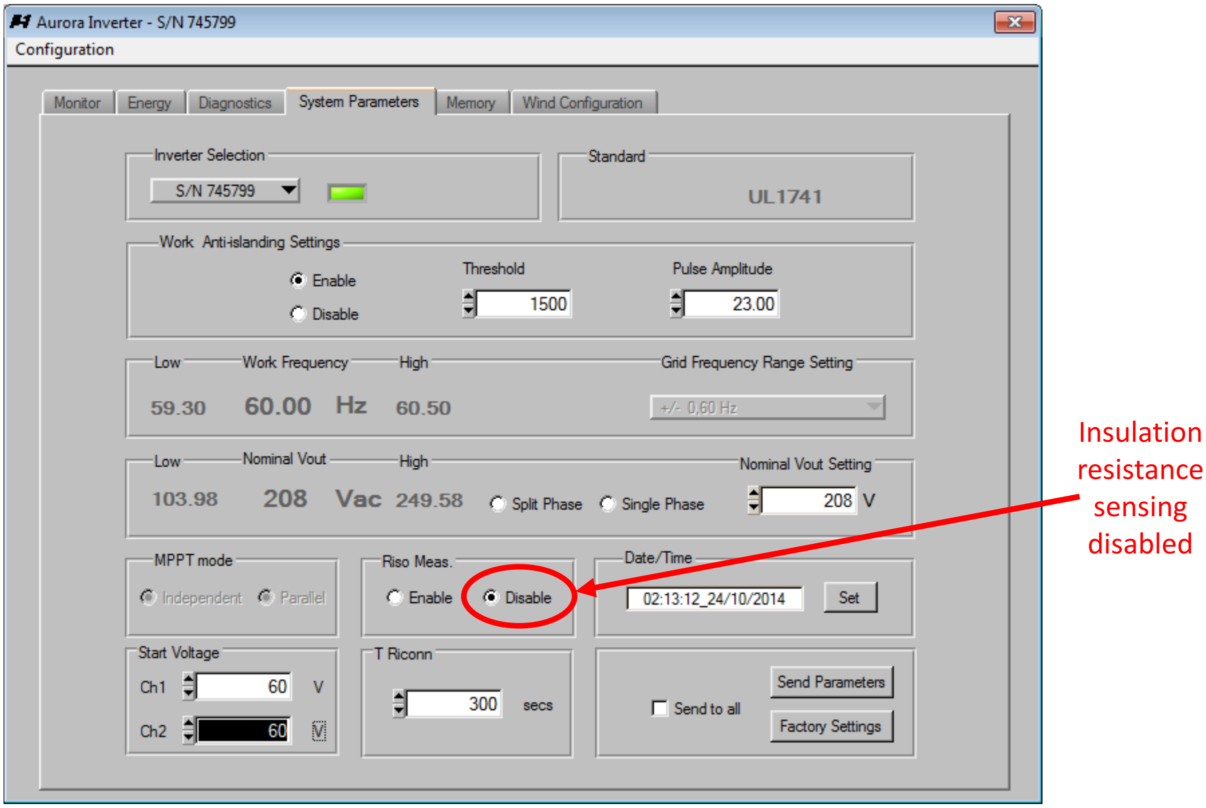

Figure 13 Aurora Installer system parameters window

4.3.2. *CompactRIO – inverter control interface*

Correct operation of the interface between the CompactRIO controller and the three inverters was verified per Section 5.3, Step 5 of the test plan. During initial configuration of the inverters, the CompactRIO control outputs were set to zero power settings (30 Hz) and their outputs were recorded with an oscilloscope. See Figure 14 showing an oscilloscope plot of the Inverter 1 control signal; the pulse frequency was 30.05 Hz. The Inverter 2 and 3 control signals were identical. This oscilloscope recording was made at the same time that the screen shot of the Aurora Installer window for Inverter 1 shown in Figure 12 was saved. The pulse frequency of the PowerOne inverter control input is displayed as the "wind frequency", 30 Hz, in Figure 12, which matches the oscilloscope measurement. The wind frequencies displayed by Aurora Installer for Inverters 2 and 3 were also 30 Hz.

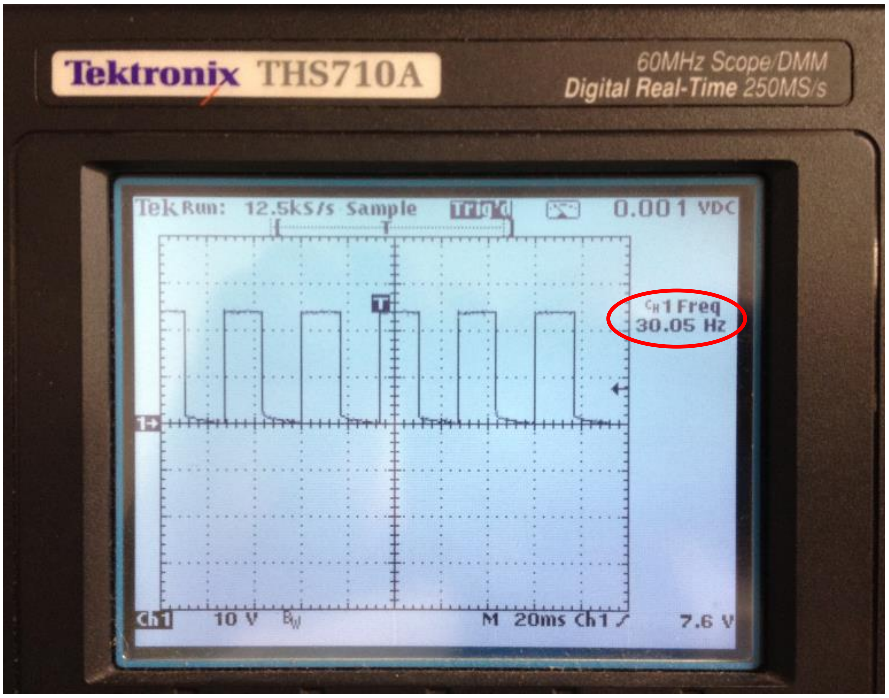

Figure 14 Oscilloscope plot of CompactRIO control output for Inverter 1

4.3.3. *Inverter input voltage measurements*

Inverter input voltage measurements made by the CompactRIO controller were checked against measurements made with a voltmeter and also internal measurements of the three inverters. The results are shown in Table 3. Measurements were made with the inverter input voltage supplied by a variable 0-110 V dc power supply adjusted for maximum voltage output. See Figure 15 for a photograph of this power supply. All measurements match within 0.3%.

Table 3 Measurements of inverter input voltage

Voltage Measurement Method	Measurement
Fluke 15B meter at variable dc supply (source)	111.8 V
CompactRIO via PT1 transducer	112.15 V
Inverter 1 (host PC via Aurora Installer)	112 V
Inverter 2 (host PC via Aurora Installer)	112 V
Inverter 3 (host PC via Aurora Installer)	112 V

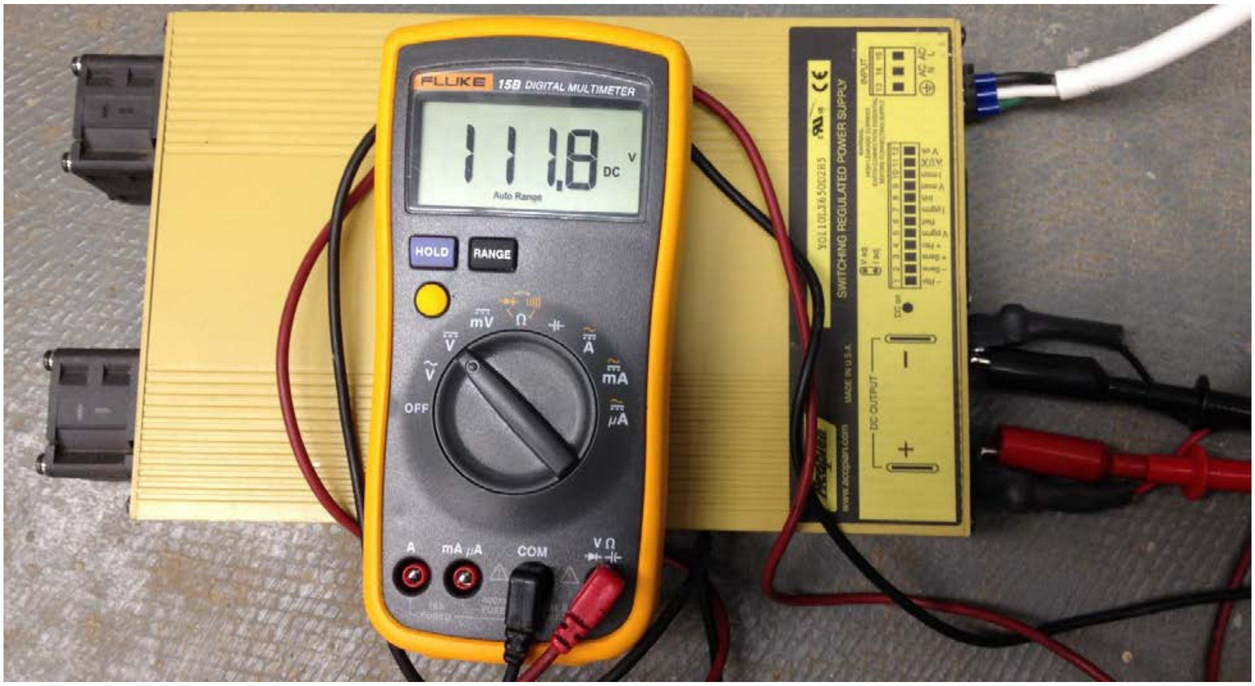

Figure 15 Acopian 0-110 Vdc power supply that was used to provide dc input power to inverters

4.3.4. *Individual low power inverter operation and inverter current measurements*

Each inverter was operated separately per Section 5.3, Steps 6 and 7 of the test plan with input voltage sourced from the Acopian power supply shown in Figure 15, adjusted for maximum output voltage (approximately 110 V). The inverters were connected to the 208 Vac grid and operated up to the maximum 6 A current capability of the Acopian power supply. Inverter dc current followed the cRIO manual current command settings input through the host PC. See Figure 16 for host PC displays of inverter input currents measured by the cRIO controller with the manual current command entered through the user interface initially set to 6 A , then changed to 3 A, then changed back to 6 A for each inverter. The currents for each of the three inverters were consistently about 0.3 A to 0.4 A higher than the cRIO manual current command. This error will not have a significant effect on operation of the device.

A comparison of current measurements made with the cRIO data acquisition, the inverter (read through Aurora Installer), and with a Fluke 336 clamp on meter are shown in Table 4 for a manual current command of 6 A. The measurements differ by about 5%, likely due to the inaccuracy of the measurements at low current. The cRIO HAL-50S, 50 A current transducer has 1% accuracy (±0.5A); the inverter measurement a 2% of inverter current rating accuracy (±0.7A), and the Fluke 336 600 A meter has a 1% accuracy (±6A). The cRIO measurement, expected to be the most accurate, indicates that the difference between the currents measured for the three inverters were less than 2%.

Figure 16 Inverter input currents for individual operation with 3A, 6A, and 3A manual current command

Table 5 Comparison of inverter input current measurements

Current	Measurement	
cRIO controller manual current command	6 A	
Inverter 1 input current	cRIO	6.4 A
	Inverter	6.2A
	Fluke 336 meter	6.6 A
Inverter 2 input current	cRIO	6.3 A
	Inverter	6.6A
	Fluke 336 meter	6.7 A
Inverter 3 input current	cRIO	6.4 A
	Inverter	6.4A
	Fluke 336 meter	6.8 A

4.3.5. *Parallel operation of three inverters*

The three inverters were operated in parallel per Section 5.3, Step 8 of the test plan. The inverter input voltage, supplied by the power supply shown in Figure 15, was left adjusted to 110 V. The cRIO current command was adjusted to 5 A; the current capability of the Acopian power supply was exceeded with higher commands. The inverter input current measurements are listed in Table 6. The cRIO current transducer measures the sum of the three inverter input currents during parallel measurement. This measurement was 6.3 A. This is consistent with the results described in Section 4.3.4 for individual inverter operation, where the input current for each inverter exceeded the command by 0.3 A to 0.4 A. Individual inverter currents were measured using the inverters and a Fluke 336 meter. As described in Section 4.3.4, these measurements are not very accurate at low current, with the inverters and Fluke 336 meter having accuracies of ±0.7 A and ±6 A, respectively. The Table 6 results indicate that the three inverters share current within at least 25% at low power.

Table 6 Inverter input current measurements for parallel inverter operation

Current	Measurement	
cRIO controller manual current command	5 A	
cRIO measurement – total inverter current	6.3 A	
Inverter 1 input current	Inverter	1.8 A
	Fluke 336 meter	2.2 A
Inverter 2 input current	Inverter	2.4 A
	Fluke 336 meter	2.1 A
Inverter 3 input current	Inverter	2.4 A
	Fluke 336 meter	2.3 A

4.4. Ground fault testing

Ground fault testing was conducted per Section 5.4 of the test plan (Appendix I). See Figure 15 for a photo of the test setup used to inject a 100 mA simulated ground fault current in the sensor, located in the dc jbox, by passing an additional wire loop through the sensor with a 330 Ω resistor connected across 24 V.

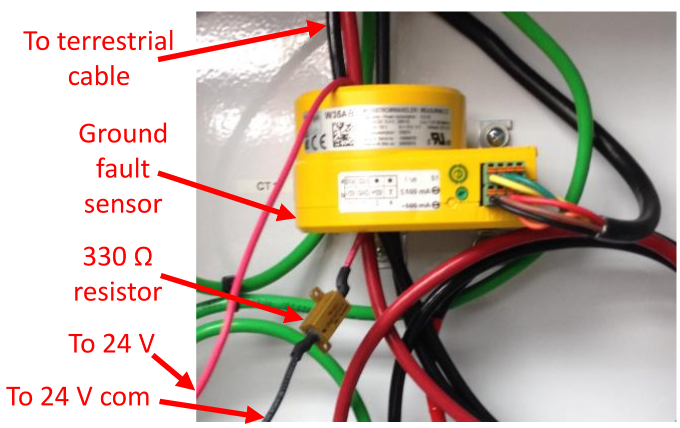

Figure 17 Setup to inject 100 mA positive current through ground fault sensor

The ground fault threshold was set to 75 mA via the cRIO user interface on the host PC. The cRIO ground fault indicator was observed along with the cRIO ground fault current measurements for both positive and negative 100 mA ground fault current. The polarity of the current was reversed by reversing the direction of the wire loop passing through the sensor, shown in Figure 15. Tests were repeated for 200 mA ground fault current by connecting a second, parallel 330 Ω resistor to double the test current. See Figure 18 for screen shots of the cRIO user interface that show the measured ground fault currents for positive current followed by zero current then negative current, for test runs with both 100 mA and 200 mA of injected current. These tests were conducted with the three inverters disconnected. The cRIO ground fault measurements are made through a Bender ground fault sensor which provides a positive measurement regardless of current direction. The result indicate that there is an offset of approximately 15 mA in the measurement that adds to positive currents and subtracts from negative currents. This is seen in results for both the 100 mA and 200 mA tests. The cRIO ground fault indication was active for both 100 mA and 200 mA ground fault currents in both directions because, even with the 15 mA offset, the readings all exceeded the 75 mA threshold. The fault indication was off while the ground fault current was zero.

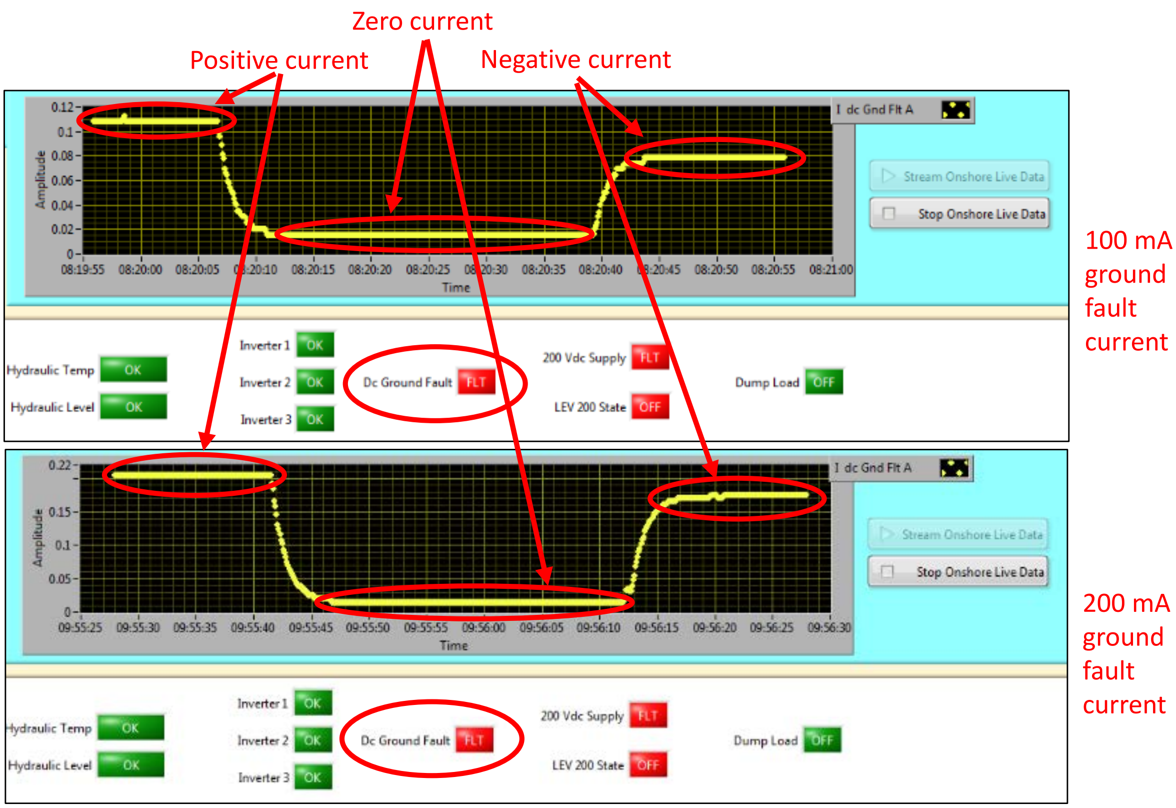

Figure 18 cRIO user interface showing results of 100 mA and 200 mA ground fault tests

The ground fault tests were not repeated with the inverters operating, as described in Section 5.4 Step 4 of the test plan, due to a faulty 125 A, 208 V circuit breaker. This circuit breaker, installed by NWEI, initially closed but would not close again (even at zero voltage) after being turned off overnight. This circuit breaker will be replaced and this test will be performed at a later date.

4.5. Dump Load Testing

Dump load testing was conducted per Section 5.5 of the test plan (Appendix I). The inverters were disabled during the test. The Acopian 0-110 V dc power supply was used to supply voltage to the 9900 µF capacitors at the inverter inputs. The dump load turn on and turn off thresholds in the cRIO control were adjusted to 100 V and 70 V, respectively, and the output current limit control for the Acopian supply was reduced to approximately 4 A this test. By limiting the power supply output current to 4 A, when the 15 Ω dump load was connected with a voltage of 100 V (the turn-on voltage threshold), voltage decreased to simulate normal operation. See the oscilloscope plots in Figure 19 for the results of this test. The top plot in Figure 19 is of the capacitor voltage, which ramps up and down between approximately 70 V and 100 V as expected. The lower plot is of the gate drive for the Insulated Gate Bipolar Transistor (IGBT), the controlled switch that turns the dump load on and off. When the gate drive is high the IGBT is turned on. At the larger 200 ms per division time scale, the gate drive signal is consistent with the expected switching action. To the right side of Figure 19 is a plot with an expanded time scale (1 µs per division) of the IGBT gate drive signal, however, which shows multiple switching of the IGBT during turn-off. This multiple switching will cause additional heating and noise emissions from the IGBT and is undesirable. A modification the gate drive circuitry will be necessary to correct this.

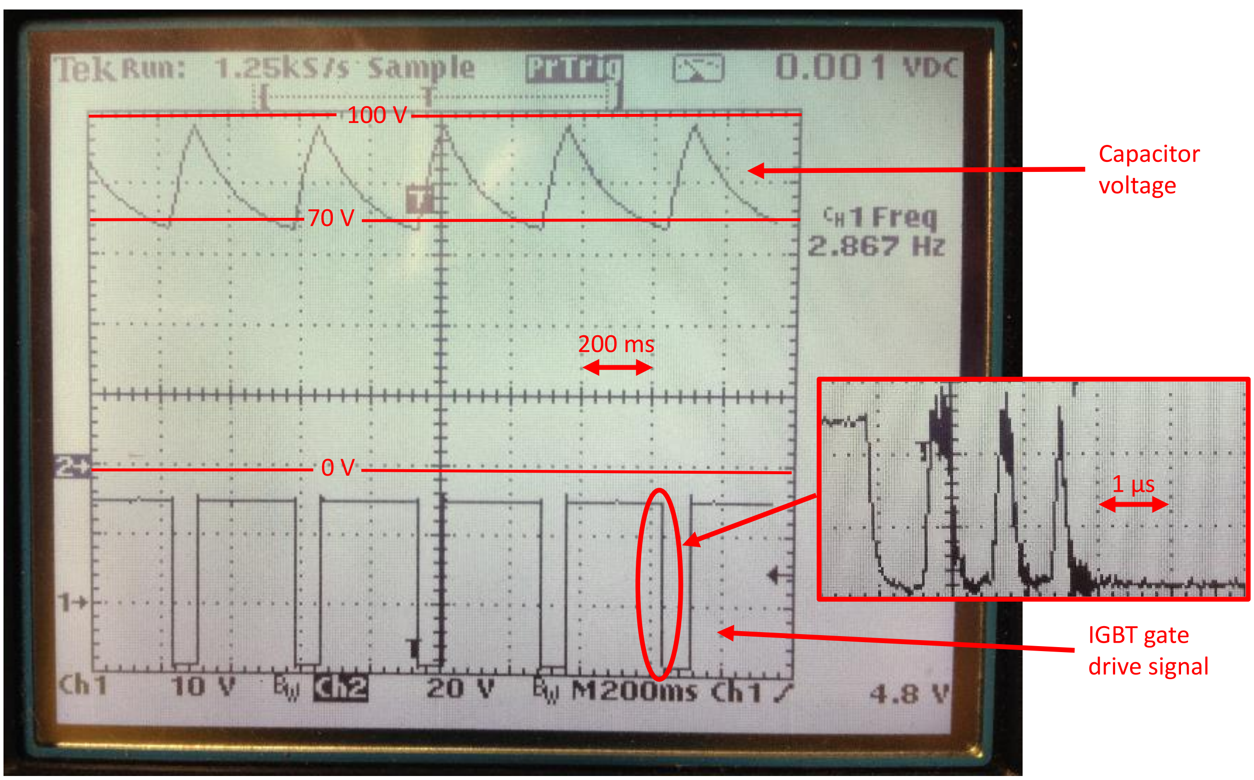

Figure 19 Oscilloscope plots showing capacitor bank voltage and IGBT gate drive during dump load tests

5. Discussion and Conclusions

These tests successfully demonstrated proper operation of the grid interconnection equipment that NWEI has installed in Building 614, Room 106 at MCBH to the extent possible before full power operation with the half-scale NWEI device. Control of the inverters was demonstrated while circulating a small amount of power (approximately 700 W) to the grid, correct function of the UPS and system power supplies was verified, the functionality of the overvoltage limiting dump load system was verified, and the ability of the system to sense and shut down in the event of a ground fault was demonstrated.

While the tests were being conducted two problems were discovered that will be corrected prior to deployment of the NWEI device: 1) the 125 A, 208 V circuit breaker installed in Room 106 was faulty, as described in Section 4.4, and 2) the dump load IGBT turns off with a “switch bounce” behavior as described in Section 4.5. The 125 A circuit breaker did not significantly affect testing because it operated properly until late in the test, and will be replaced. The dump load IGBT problem is due to a slow signal from a solid state relay used in the gate drive circuit. This IO-ODC-60-LL relay, shown at the top of Figure 20, is used to interface the 0-24V dump load control signal from the cRIO to the 0-5V signal needed at the input to the gate driver for the dump load IGBT. It will be replaced by the active circuit shown at the bottom of Figure 20 before the NWEI device is deployed. That circuit, to be built in a small DIN-rail mount box and installed in the NWEI electrical equipment enclosure, uses a much faster, more noise immune component recommended by the manufacturer of the gate driver and is expected to correct the problem.

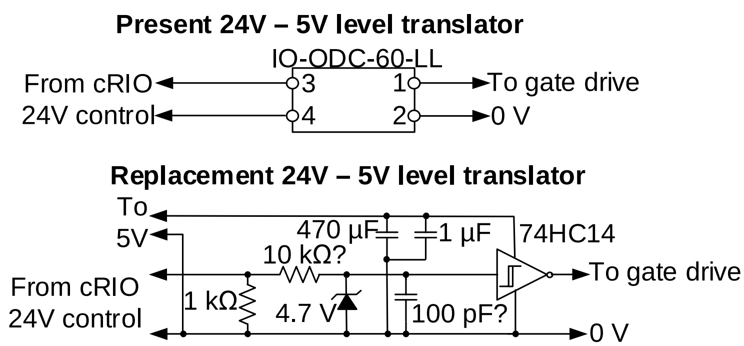

Figure 20 Present dump load IGBT level translator and future replacement to correct multiple switching

Some aspects of the equipment operation can only be tested at higher power after the NWEI device is deployed. Thermal measurements will be made to check that the air conditioning in Room 106 can keep up with the heat loss from the inverters and other equipment when the NWEI device outputs full power. Equal current and power sharing between the three parallel inverters is most important at full power, and this will be verified. Testing of the dump load system will be performed during high power output of the NWEI device to verify proper IGBT switching at higher voltages and the ability of the dump load resistor to limit the voltage output of the device. These tests will be performed immediately after device deployment to follow up on the low power testing described in this document.

APPENDICES

Appendix I – Test Plan

Appendix II – Electrical Drawing, NWEI Bunker Equipment